In the Claims:

The pending claims are presented below.

1. (Original) A memory cell comprising:

a thyristor device including doped regions of opposite polarity;

a first word line providing read and write access to the memory cell; and

a second word line located adjacent to and separated by an insulative material from at least one of the doped regions of the thyristor device and used for write operation to the memory cell by enhancing the switching of the thyristor device from a high conductance state to a low conductance state and from the low conductance state to the high conductance state.

2. (Original) The memory cell of claim 1, further comprising a transistor, wherein the read and write access is provided by the transistor with its gate forming at least part of the first word line.

3. (Original) The memory cell of claim 2, wherein the transistor is a MOSFET transistor.

4. (Original) The memory cell of claim 1, wherein the second word line enhances the switching of the thyristor device by substantially improving the switching speed of the thyristor device from the high conductance state to the low conductance state.

5. (Original) The memory cell of claim 1, wherein the second word line is adapted to enhance the switching of the thyristor device by substantially reducing the voltage requirement of the thyristor device for switching from the low conductance state to the high conductance state.

6. (Original) The memory cell of claim 1, wherein at least part of the cell is arranged in a vertical configuration extending above a substrate surface.

7. (Original) The memory cell of claim 1, wherein at least part of the cell is arranged in a vertical configuration extending below a substrate surface.

8. (Original) The memory cell of claim 1, wherein at least part of the cell is arranged in a planar configuration parallel to a substrate surface.

9. (Original) The memory cell of claim 8, wherein the substrate surface is part of a silicon-on-insulator substrate.

10. (Original) The memory cell of claim 2, wherein the transistor and the thyristor device are arranged in a planar configuration parallel to a substrate surface.

11. (Original) The memory cell of claim 10, wherein the substrate surface is part of a silicon-on-insulator substrate.

12. (Original) A memory array comprising:

a first and a second word line; and

a plurality of memory cells, each memory cell comprising a thyristor device including doped regions of opposite polarity, wherein

the first word line providing read and write access to the memory cell; and

a portion of the second word line located adjacent to and separated by an insulative material from at least one of the doped regions of the thyristor device and used for write operation to the memory cell by enhancing the switching of the thyristor device from a high conductance state to a low conductance state and from the low conductance state to the high conductance state.

13. (Original) The memory array of claim 12, wherein the memory cell further comprises a transistor, and wherein the read and write access is provided by the transistor with its gate forming at least part of the first word line.

14. (Original) The memory array of claim 13, wherein the transistor is a MOSFET transistor.

15. (Original) The memory array of claim 12, wherein the second word line enhances the switching of the thyristor device by substantially improving the switching speed of the thyristor device from the high conductance state to the low conductance state.

16. (Original) The memory array of claim 12, wherein the second word line enhances the switching of the thyristor device by substantially reducing the voltage requirement of the thyristor device for switching from the low conductance state to the high conductance state.

17. (Original) The memory array of claim 12, wherein at least part of the memory cell is arranged in a vertical configuration extending above a substrate surface.

18. (Original) The memory array of claim 12, wherein at least part of the memory cell is arranged in a vertical configuration extending below a substrate surface.

19. (Original) The memory array of claim 12, wherein at least part of the memory cell is arranged in a planar configuration parallel to a substrate surface.

20. (Original) The memory array of claim 19, wherein the substrate surface is part of a silicon-on-insulator substrate.

21. (Original) The memory array of claim 13, wherein the transistor and the thyristor device are arranged in a planar configuration parallel to a substrate surface.

22. (Original) The memory array of claim 21, wherein the substrate surface is part of a silicon-on-insulator substrate.